ARRAY OF CELLS INCLUDING A SELECTION BIPOLAR TRANSISTOR AND FABRICATION METHOD THEREOF

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an array of cells including a selection bipolar transistor and a fabrication method thereof. In particular, the invention refers to a cell array of a phase change memory (PCM) device, without being limited thereto.

Description of the Related Art

As is known, phase change memory cells utilize a class of materials that have the unique property of being reversibly switchable from one phase to another with measurable distinct resistivity. Specific materials that may be suitably used in phase change memory cells are alloys of elements of the VI group of the periodic table as Te or Se, also called chalcogenides or chalcogenic materials. Thus a thin film of chalcogenic material may be employed as a programmable resistor, switching between a high and a low resistance condition.

The use of chalcogenic storage elements has been already proposed to form a memory cell. To avoid disturbances caused by adjacent memory cells, the chalcogenic element is generally coupled with a selection element, generally a MOS transistor or a diode.

A possible organization of a PCM array is shown in Figure 1. The memory array 1 of Figure 1 comprises a plurality of memory cells 2, each including a storage element 3 of the phase change type and a selection element 4 formed as a bipolar PNP transistor. The same architecture may be however used for any array of storage elements that are selectively addressed through respective bipolar transistor selection elements.

The memory cells 2 are arranged on rows and columns. In each memory cell 2, the storage element 3 has a first terminal connected to an own bit line BLn-1, BLn, BLn+1, ..., and a second terminal connected to an emitter of an own bipolar transistor 4; the bipolar transistor 4 has a base connected to an own control line, also called word line WLn-1, WLn, WLn+1, ... and a grounded collector.

In order to address the storage element 3 belonging to a specific cell 2, for example the one connected to bit line BLn and to world line WLn, the bit line connected to the addressed cell (selected bit line BLn) is biased at a high voltage V_{OP} and all the other (unselected) bit lines BLn-1, BLn+1, ... are grounded. Furthermore, the word line connected to the addressed cell (selected word line WLn) is grounded and all the other (unselected) word lines WLn-1, WLn+1, ... are biased at V_{CC}, so that the bipolar transistors 4 not connected to the selected word line are held off.

CMOS compatible processes for manufacturing PCM have been already proposed. For example, U.S. patent application N. 10/313,991, filed on December 5, 2002 and entitled Small Area Contact Region, High Efficiency Phase Change Memory Cell and Fabrication Method Thereof, which is incorporated by reference herein in its entirety, describes a process providing a small area contact between the chalcogenic region and the resistive electrode. In this prior patent application, each cell is housed in an own active area. This prior application however does not deal with the optimization of the layout of the memory cell.

Since electronic devices are required to be more and more compact, it is desired to provide a highly compact layout for the array structure of Figure 1.

BRIEF SUMMARY OF THE INVENTION

To increase the compactness of the array, according to one aspect of the invention, at least two cells are housed in a same active area of the device.

In particular, according to an embodiment, strips of active area are provided, each strip housing a plurality of emitter regions and base contact regions of a plurality of selection bipolar transistors, with the emitter regions and the base contact regions arranged alternately.

According to another embodiment, each active area has a rectangular shape and houses at least one base contact region and two emitter regions, so that at least two cells are arranged in the same active areas.

According to a further embodiment, strips of active area are provided, each strip housing a plurality of emitter regions and base contact regions of a plurality of selection bipolar transistors, at least two emitter regions being arranged between two subsequent base contact regions.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

For the understanding of the present invention, preferred embodiments are now described, purely as non-limitative examples, with reference to the enclosed drawings, wherein:

Figure 1 is a circuit diagram of an array of cells including a storage element and a selection bipolar transistor;

Figure 2 shows the masks used for a cell array according to a first embodiment of the invention;

Figure 3 shows a cross-section of the first embodiment, taken along line III-III of Figure 2;

Figure 4 shows a cross-section of the first embodiment, taken along line IV-IV of Figure 2;

Figure 5 shows the masks used for a cell array according to a second embodiment of the invention;

Figure 6 is a cross-section of the second embodiment, taken along line VI-VI of Figure 5;

Figure 7 shows the masks used for a cell array according to a third embodiment of the invention; and

Figure 8 is a cross-section of the third embodiment, taken along line VIII-VIII of Figure 7.

DETAILED DESCRIPTION OF THE INVENTION

According to the embodiment of Figures 2-4, a memory array is formed in a body 10 of semiconductor material including a P-type common collector region 11. As visible in particular from Figure 4, the body 10 houses a plurality of active area strips 12, of N-type, defining base regions. The active area strips 12 extend parallel to each other along a first direction (X-direction) and are electrically insulated from each other by field oxide regions 13 (Figure 4).

Each active area strip 12 accommodates a plurality of emitter regions 14, of P^+-type, and plurality of base contact regions 15, of N^+-type, that are arranged alternately, that is each emitter region 14 is arranged between two base contact regions 15, and each base contact region 15 is arranged between two emitter regions 14. Thus, each pair of regions including an emitter region 14 and the adjacent base contact region 15 (for example, an emitter region 14 and the base contact region 15 arranged on right thereof), the active area strip 12 they are accommodated in, and the underlying collector region 11 form a selection transistor 20 of PNP-type, corresponding to bipolar transistor 4 of Figure 1.

A dielectric region 21 extends on the body 10 and accommodates contacts, storage elements and interconnection lines. The dielectric region 21 is generally formed by more layers deposited subsequently to allow forming the various regions therein and may also include different materials.

First and second contacts 22, 23 extend in first and second openings 27a, 27b of the dielectric region 21. Preferably, the first and second contacts 22, 23 are of tungsten, covered on the vertical and bottom sides with a barrier material (for example, Ti/TiN), not shown for simplicity.

The first contacts 22 extend each from an emitter region 14 to a chalcogenic storage element 24 forming the storage element 3 of Figure 1. First metal lines 25, forming bit lines corresponding to bit lines BLn-1, BLn, BLn+1 of Figure 1, extend along a second direction (Y-direction), thus transversely to the active area strips 12. Each first metal line 25 is in contact with the chalcogenic storage elements 24 that are aligned in the Y direction, as visible from the cross-section of Figure 4. The first metal lines 25 are formed preferably in a first metal level.

The second contacts 23 are higher than the first contacts 22 and extend each from a base contact region 15 to second metal lines 26. The second metal lines 26, forming word lines corresponding to word lines WLn-1, WLn, WLn+1 of Figure 1, extend along the first direction (X-direction), thus parallel to the active area strips 12 and perpendicular to the first metal lines 25. Each second metal line 25 is in contact with the second contacts 23 that are aligned in the X direction, as visible from the cross-section of Figure 3. The second metal lines 26 are formed preferably in a second metal level.

Figure 2 shows some masks to be used for manufacturing the memory array of Figures 3 and 4. In particular, Figure 2 shows an active area mask 30, a contact mask 31 and an emitter mask 32.

The process for manufacturing the memory array of Figures 3 and 4 is the following.

Initially, the field oxide regions 13 are grown in the body 10, preferably including a substrate and an epitaxial layer of P type, using the active area mask 30 of Figure 2, and thus defining the active area strips 12.

Then the active area strips 12 are implanted with N-type doping agents, thus forming the base regions of bipolar transistors. The body 10 is covered by a first layer of insulating material, forming the bottom portion of the dielectric region 21, and contacts are opened using contact mask 31, forming the first openings 27a and the bottom portion of the second openings 27b. Then, a

boron implant (P+ emitter implant) is made, using emitter mask 32, so as to form emitter regions 14 below the first contacts 22. Thereafter, using an own mask not shown, that is the negative of the emitter mask 32, base contact regions 15 are implanted below the second contacts 23. In case, the base contact regions 15 may be doped before the emitter regions 14.

Then the first openings 27a and the bottom part of the second openings 27b are filled with a barrier layer, *e.g.*, Ti/TiN, and with tungsten; then chalcogenic storage elements 24, the first metal lines 25, the second metal lines 26, the upper portion of the dielectric region 21 and the upper portion of the second contacts 23 are formed, *e.g.*, as described in the before mentioned U.S. patent application N. 10/313,991.

Alternatively, instead of the chalcogenic storage elements 24, other storage elements or other two or three-terminal elements that are compatible with standard CMOS back-end processes may be formed.

According to a different embodiment, a doped region 28 of N type, having a doping level close to that of the active area strips 12, is formed below each emitter region 14, as shown by broken lines in Figure 3. In this case an N-type conductivity determining agent is implanted using the emitter mask 32, just after or just before the P+ emitter implant. Thereby, the base resistance and thus the emitter-to-base voltage drop are reduced, increasing also the immunity of the bipolar transistor against emitter-to-collector leakage and punch-through.

The embodiment of Figures 2-4 has the following advantages. First, the cell array has a very compact layout, thus reducing the overall dimensions of the device comprising the array. Furthermore, no active area corners are present inside the array, thus reducing to a minimum the stress due to isolation. There is also an intrinsic redundancy of the base contacts; the solution ensures both reduced defects and reduced intrinsic current leakage; thus the array has very good electronic properties.

Figures 5 and 6 show a different embodiment, wherein, in the X-direction, each emitter region 14 is separated by the adjacent emitter regions 14 by a base contact region 15 on one side (left in the drawings), and by a field oxide region 40 on the other side (right in the drawings). Here, the active area mask 41 (Figure 5) has an grid-like pattern, and a field oxide region 40 having a grid-like shape, delimits a plurality of active regions 42 of rectangular shape. Each active region 42 accommodates only one base contact region 15 and two emitter regions 40, arranged on different sides of the base contact region 15 in the X-direction. Thus, each active region 42 accommodate two bipolar transistors 43 that share a same base contact region 15.

The cross-section in a plane perpendicular to that of Figure 6 is the same as in Figure 4.

As visible from Figure 5, the shape of the active area mask 41 and of the emitter mask 44 differ from the active area mask 30 and the emitter mask 32 of Figure 2; however, contact mask 31 is about the same as in Figure 2.

The manufacturing process of the memory array of Figures 5 and 6 is the same described above with reference to Figures 2-4, with the only exception of the shape of the active area mask 41 and the emitter mask 44, as above outlined.

Also in the embodiment of Figures 5 and 6 a N-doped region 28 (not shown) may be provided below each emitter region 14, to reduce the base resistance.

With the embodiment of Figures 5 and 6, it is possible to save around 20% of silicon area with respect to the embodiment of Figures 2-4, even if the active area corners could introduce defectivity issues.

Figures 7 and 8 show a third embodiment, wherein adjacent emitter regions 14 are not separated by other formations (base contacts or insulating material), but their electrical separation is only ensured by the intrinsic base region (active area strips 12).

Specifically, here the active areas are formed as active area strips 12, analogously to the embodiment of Figures 2-4, but each base contact 15 is formed every two emitter regions 14, analogously to the embodiment of Figures 5 and 6. Thus, each base contact region 15 forms two bipolar transistors 50 with the adjacent emitter regions 14.

The masks used to obtain the structure of Figure 8 are shown in Figure 7: as may be noted, the active area mask 30 is the same as in Figure 2 and the emitter mask 44 is the same as in figure 5.

The manufacturing process of the memory array of Figures 7 and 8 is the same described above with reference to Figures 2-4, with the only exception of the shape of the emitter mask 44, as above outlined.

In the embodiment of Figures 7 and 8, it is possible to further reduce the area occupation, depending on the minimum distance attainable between two adjacent emitter regions 14; however, the presence of lateral parasitic PNP bipolar transistors (formed by two adjacent emitter regions 14 and the intermediate portion of the respective active area strip 12) renders this embodiment applicable only to solutions including design measure to reduce the resulting leakage current.

According to a different embodiment, more than two emitter regions 14, *e.g.*, four, eight, etc., may be arranged between consecutive base contact regions 15 without an oxide or base isolation between them. In this case, the area occupation is still reduced, but the current leakage problem is worsened and base resistance could become a limiting factor for the emitters located farther from the base contact.

The advantages of the present invention are clear from the above.

Finally, it is clear that numerous variations and modifications may be made to the cell array as described and illustrated herein, all falling within the scope of the invention as defined in the attached claims.

E.g., it is possible to arrange multiple emitter regions 14 at each side of a base contact region 15 also in the embodiments of Figures 2-4 and 5-6, thus

reducing the area occupation, while worsening current leakage due to parasitic components.

Furthermore, as indicated, the same array layout may be used for cells including a different storage component.

All of the above U.S. patents, U.S. patent application publications, U.S. patent applications, foreign patents, foreign patent applications and non-patent publications referred to in this specification and/or listed in the Application Data Sheet, are incorporated herein by reference, in their entirety.